together, these changes increase the internal I/O bandwidth by at least a factor of 8. Four internal buses are used to route these internal I/O lines. Increasing the number of I/O lines and then splitting them in the middle greatly reduces the capacitance of each internal I/O line which in turn reduces the column access time, increasing the column access bandwidth even further.

**IN THE CLAIMS:**

Kindly **cancel** claims 1-150, without prejudice.

Kindly **add** the following claims:

151. (New) A synchronous integrated circuit device having a memory array which includes dynamic random access memory cells, wherein the integrated circuit device comprises:

a clock receiver to receive an external clock signal;

a plurality of sense amplifiers, coupled to the memory array, to sense data from the dynamic random access memory cells; and

a plurality of input receivers to sample an operation code synchronously with respect to a transition of the external clock signal, the operation code including precharge information, wherein, in response to the precharge information, the plurality of sense amplifiers is automatically precharged after the data is sensed.

152. (New) The integrated circuit device of claim 151 wherein the operation code specifies a read operation, and wherein the integrated circuit device further includes a plurality of output drivers to output first and second portions of the data in response to the operation code specifying a read operation.

153. (New) The integrated circuit device of claim 152 wherein:

the plurality of output drivers output the first portion of the data synchronously with respect to a rising edge transition of the external clock signal; and

the plurality of output drivers output a second portion of the data synchronously with respect to a falling edge transition of the external clock signal.

154. (New) The integrated circuit device of claim 153 further including a delay lock loop, coupled to the plurality of output drivers, to synchronize the output of the first and second portions of the data with the external clock signal.

155. (New) The integrated circuit device of claim 153 further including a plurality of multiplexers, wherein each multiplexer of the plurality of multiplexers is coupled to an output driver of the plurality of output drivers.

156. (New) The integrated circuit device of claim 155 wherein:

the plurality of multiplexers provide the first portion of the data to the plurality of output drivers in response to a rising transition of the external clock signal; and

the plurality of multiplexers provide the second portion of the data to the plurality of output drivers in response to a falling edge transition of the external clock signal.

157. (New) The integrated circuit device of claim 151 wherein the plurality of input receivers further includes a first input receiver to sample a first bit of the operation code synchronously with respect to the transition of the external clock signal, wherein the precharge information is encoded in the first bit of the operation code.

158. (New) The integrated circuit device of claim 157 wherein the plurality of input receivers further includes a second input receiver to sample a second bit of the operation code synchronously with respect to the transition of the external clock signal, wherein the second bit of the operation code specifies a read operation, wherein a portion of the data is output from the integrated circuit device in response to the second bit of the operation code specifying the read operation.

~~159. (New) The integrated circuit device of claim 158 wherein the plurality of~~ input receivers further includes a third input receiver to sample address information synchronously with respect to the external clock signal.

160. (New) The integrated circuit device of claim 151 wherein the operation code includes a plurality of bits, and wherein the plurality of bits, in combination, encodes information which specifies that the plurality of sense amplifiers sense the data from the memory array.

161. (New) The integrated circuit device of claim 151 further including row decoder circuitry, coupled to the memory array, to identify, in response to a row address, a row of the memory array that stores the data to be sensed by the plurality of sense amplifiers.

162. (New) The integrated circuit device of claim 151 further including column decoder circuitry, coupled to the plurality of sense amplifiers, to identify, in response to a column address, a portion of the data.

163. (New) The integrated circuit device of claim 151 further including a clock synchronization circuit coupled to the clock receiver, wherein the clock synchronization circuit includes:

a delay line to generate an internal clock signal, wherein the internal clock signal has a delay with respect to the external clock signal; and

a comparator to compare the internal clock signal with the external clock signal, wherein the delay of the internal clock signal is adjusted based on the comparison between the internal clock signal and the external clock signal.

164. (New) The integrated circuit device of claim 163 further including a plurality of output drivers to output first and second portions of the data in response to the operation code specifying a read operation, wherein the clock synchronization circuit is coupled to the plurality of output drivers to synchronize the output of the first and second portions of the data with the internal clock signal.

165. (New) The integrated circuit device of claim 164 wherein the plurality of input receivers samples the operation code from a plurality of external signal lines of an external bus, wherein the external bus is used to carry, in a multiplexed format, the operation code, and the first and second portions of the data.

166. ~~(New) A synchro~~nous integrated circuit memory device including an array of memory cells, wherein the memory device comprises:

a clock receiver to receive an external clock signal;

a plurality of sense amplifiers, coupled to the array of memory cells, to sense data, wherein a portion of the data is output from the memory device in response to a first operation code bit specifying a read operation;

a first input receiver to sample the first operation code bit in response to a first transition of the external clock signal;

a second input receiver to sample a second operation code bit in response to the first transition of the external clock signal, wherein the second operation code bit indicates whether precharging the plurality of sense amplifiers occurs automatically after the data has been sensed; and

a plurality of output drivers to output the portion of the data synchronously with respect to the external clock signal.

167. (New) The memory device of claim 166 wherein the second input receiver further samples an address bit synchronously with respect to a second transition of the external clock signal.

168. (New) The memory device of claim 166 wherein the plurality of output drivers output the portion of the data onto an external bus, the external bus including a plurality of external signal lines.

169. ~~(New) The memory device of claim 168 wherein:~~

the first operation code bit is sampled from a first signal line of the plurality of external signal lines; and

the second operation code bit is sampled from a second signal line of the plurality of external signal lines.

170. (New) The memory device of claim 169 wherein the plurality of external signal lines is used to carry, in a multiplexed format, address information and the portion of the data.

171. (New) The memory device of claim 166 further including a delay locked loop, coupled to the clock receiver, to generate an internal clock signal using the external clock signal, wherein the plurality of output drivers output the portion of the data in response to the internal clock signal.

172. (New) The memory device of claim 166 further including:

row decoder circuitry, coupled to the array of memory cells, to identify a row of the array of memory cells that stores the data to be sensed by the plurality of sense amplifiers; and

column decoder circuitry, coupled to the array of memory cells, to identify the portion of the data.

173. (New) A method of operation of a synchronous integrated circuit memory device, wherein the memory device includes an array of memory cells, wherein the method of operation of the memory device comprises:

sampling an operation code in response to a first transition of an external clock signal, wherein the operation code specifies a read operation and includes precharge information;

sensing data in a plurality of sense amplifiers, wherein the data is output in response to the operation code specifying the read operation;

automatically precharging the plurality of sense amplifiers in response to the precharge information, wherein the plurality of sense amplifiers is automatically precharged after the data is sensed; and

outputting the data synchronously with respect to the external clock signal.

174. (New) The method of claim 173 further including sampling address information synchronously with respect to the external clock signal.

175. (New) The method of claim 174 wherein the operation code and the address information are included in a request packet.

176. (New) The method of claim 174 wherein the operation code and the address information are sampled from an external bus, wherein the external bus includes a plurality of signal lines to carry the address information and the operation code in a multiplexed format.

177. ~~(New)~~ The method of claim 176 wherein the data is output onto the plurality of signal lines.

178. (New) The method of claim 173 further including:

selecting a row of memory cell locations in accordance with a first address portion; and

sensing data, from the selected row of memory cell locations, in a row of sense amplifiers, wherein the plurality of sense amplifiers is included in the row of sense amplifiers.

179. (New) The method of claim 178 further including identifying the plurality of sense amplifiers based on a second address portion.

180. (New) The method of claim 173 further including generating an internal clock signal using a delay locked loop, wherein the data is output in response to the internal clock signal.

181. (New) The method of claim 173 wherein a first portion of the data is output synchronously with respect to a rising edge transition of the external clock signal, and a second portion of the data is output synchronously with respect to a falling edge transition of the external clock signal.

182. ~~(New) A~~ method of controlling a synchronous memory device, wherein the memory device includes a plurality of sense amplifiers coupled to a memory cell array, wherein the method of controlling the memory device comprises:

providing a first operation code to the memory device, wherein the first operation code indicates that the memory device:

output data read from the memory cell array; and

precharge sense amplifiers used in reading the data from the memory cell array, wherein the sense amplifiers used in reading the data are precharged automatically after the data is read from the memory cell array; and

receiving the data from the memory device, the memory device outputting the data in response to the first operation code.

183. (New) The method of claim 182 wherein the first operation code is included in a request packet.

184. (New) The method of claim 182 further including providing a second operation code to the memory device, wherein the second operation code instructs the memory device to:

input data to be written to the memory cell array;

write the input data to the memory cell array using sense amplifiers of the plurality of sense amplifiers; and

precharge the sense amplifiers used in writing the input data to the memory cell array, wherein the sense amplifiers are precharged automatically after the input data is written to the memory cell array.

185. (~~New~~) The method of claim 184 further including:

providing, to the memory device, a row address and a column address; and

providing a third operation code to the memory device, wherein the third operation code instructs the memory device to:

output data read from a specified location of the memory cell array, wherein the specified location is identified by the row address and the column address; and

retaining, in at least a portion of the plurality of sense amplifiers, the data read from the specified location of the memory cell array.

186. (New) The method of claim 182 further including:

providing, to the memory device, a row address and a column address; and

providing a second operation code to the memory device, wherein the second operation code includes a plurality of bits, wherein the plurality of bits, in combination, encodes information which indicates that the memory device sense data from a specified location of the memory cell array using at least a portion of the plurality of sense amplifiers, wherein the specified location is identified by the row address and the column address.

187. (New) The method of claim 182 further including providing address information to the memory device, wherein the address information is provided synchronously with respect to the external clock signal.

188. (New) The method of claim 187 wherein the address information and the first operation code are issued to the memory device via an external bus.

189. (New) A synchronous memory device having a memory array which includes dynamic memory cells, wherein the memory device comprises:

a plurality of sense amplifiers, coupled to the memory array, to sense data from the dynamic memory cells; and

a plurality of input receivers to sample an operation code synchronously with respect to a transition of an external clock signal, the operation code including precharge information, wherein, in response to the precharge information, the plurality of sense amplifiers are automatically precharged after the data is sensed;

a plurality of output drivers to output first and second portions of the data in response to the operation code specifying a read operation; and

a delay locked loop, coupled to the plurality of output drivers, to synchronize the output of the first and second portions of the data with the external clock signal.

190. (New) The memory device of claim 189 wherein:

the plurality of output drivers output the first portion of the data synchronously with respect to a rising edge transition of the external clock signal; and

the plurality of output drivers output the second portion of the data synchronously with respect to a falling edge transition of the external clock signal.

191. ~~(New) The memory device of~~ claim 189 further including a plurality of multiplexers, wherein each multiplexer of the plurality of multiplexers is coupled to an output driver of the plurality of output drivers.

192. (New) The memory device of claim 191 wherein the plurality of multiplexers provide the first portion of the data to the plurality of output drivers in response to a rising transition of the external clock signal and the plurality of multiplexers provide the second portion of the data to the plurality of output drivers in response to a falling edge transition of the external clock signal

193. (New) The memory device of claim 189 wherein the plurality of input receivers further includes a first input receiver to sample a first bit of the operation code synchronously with respect to the transition of the external clock signal, wherein the precharge information is encoded in the first bit of the operation code.

194. (New) The memory device of claim 193 wherein the plurality of input receivers further includes a second input receiver to sample a second bit of the operation code synchronously with respect to the transition of the external clock signal, wherein an encoding of the second bit of the operation code specifies the read operation.

195. (~~New) The~~ memory device of claim 189 wherein the delay locked loop includes:

a delay line to generate an internal clock signal, wherein the internal clock signal has a delay with respect to the external clock signal; and

a comparator to compare the internal clock signal with the external clock signal, wherein the delay of the internal clock signal is adjusted based on the comparison between the internal clock signal and the external clock signal.